UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE
DEPARTMENT OF ELECTRONIC ENGINEERING

2006
MAIN EXAMINATION

Title of the Paper: **ELECTRONICS II**
Course Number: **E440, PAPER 1**
Time Allowed: **Three Hours**.

Instructions:
1. To answer, pick any five out of six questions in the following pages.
2. Each question carriers 20 points.
3. This paper has 7 pages, including this page.

DO NOT OPEN THE PAPER
UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

Boolean Function Fundamentals:

Q1a 5pts: Transform the following Boolean function into K-map:

$F(A,B,C,D,E) = AB + \overline{C}D\overline{E}$.

Q1b 15pts: Using the tabulation method, simplify the following Boolean function F into either sum of products or product of sums, (not both):

$F(u, v, w, x, y) = \Sigma(0, 4, 9, B, C, D, F, 10, 14, 1D, 1F)_{hex}$

(hex number in the brackets of the above function)

Q2a 10pts: With the help of K-map, obtain the simplified expressions in (1) SOP and (2) POS of the one of the following two Boolean Functions: (you are allowed to choose only one function and obtain the two expressions of the one you picked)

$G(A,B,C,D) = \overline{A}\overline{B}\overline{C} + A\overline{B}D + \overline{A}\overline{B}C\overline{D} + ABC$

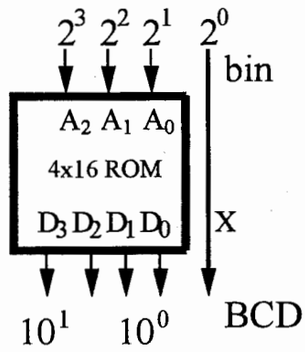
$F(A,B,C,D) = (\overline{A} + \overline{B} + D)(A + C + \overline{D})(A + \overline{B} + C + D)(\overline{A} + \overline{D})$

Q2b 10pts: Implement the Boolean function below with only NAND gates and nothing but NAND gates, yet complement inputs are available only at input terminals nowhere else. The implementation must have its function support.

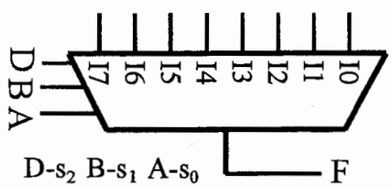
$F(A,B,C,D) = (A + \overline{B})(A + CD) + \overline{A}\overline{B}\overline{C}$

Combinational Logic Circuit:

Q3a 10pts: The 4x16 ROM together with the 2^0 line as shown in the figure below converts a 4-bit binary number to its corresponding 2-digit BCD number. Specify the ROM table for the ROM. (hint: binary1111 converts to BCD 1, $0101=15_{dec.}$)



Q3b 10pts: Implement the Boolean function below with an 8-1 multiplexer with D, B, and A connected to the address lines s_2, s_1, and s_0 respectively. $F(A,B,C,D)=\Sigma(0, 1, 2, 4, 7, 8, 12,13,15)$



Sequential Logic Circuit:

Q4 20pts: A sequential circuit is described by the following state equations; it has 3 ff's, A, B, and C, and 1 input, x. Design the sequential circuit. Use JK flip-flops to obtain a logic circuit, a state table, a state diagram, and ff input functions. (hint: missing term may be replaced by 0*Q(t))

$$A(t+1) = x\overline{B} + AB$$

$$B(t+1) = xA\overline{B}C$$

$$C(t+1) = \overline{x}B + \overline{A}B + BC$$

Registry Logical Circuit:

Q5 20pts: The operation of the addition of two n-bit signed binary numbers is specified by the following statement:

T: $A \leftarrow A+B$, $V \leftarrow C_n+C_{n-1}$

In the statement, register A holds the augend, with the sign bit in position A_n; register B holds the addend, with sign bit in B_n. The addition is performed in an n-bit parallel adder, in which the nth bit is for the addition of sign bit. Then, C_{n-1} is the carry from the addition of the two magnitudes of n-1 bit (from the (n-1)th adder), and C_n is the carry from the addition of the two sign bits (from the nth adder). The nth bit adder must be shown explicitly to make C_n visible. V in the statement is an overflow memory.

Design a registry circuit which will perform this statement.

ASM Logic Circuit:

Q6 20pts Design a finite state machine, with no restriction on the use of any logic components. Its ASM diagram is shown below. Obtain a state transition table and a circuit diagram plus the support of the logic equations. D-ff's are proper to use.

ASM diagram